Effect of Bit-Level Correlation in Stochastic Computing

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Abstract—Simple stochastic logic gates can compute complex functions using stochastic computing. A stochastic number is encoded by a unary bit stream where each bit is 0 or 1. The value of the number is represented by the percent of 1’s in the number, and is interpreted as a probability. Each bit of the stochastic number can be modeled as a Bernoulli random variable, and each stochastic number can be represented by a binomial random variable. The variance of a stochastic number is given by \( \frac{p(1-p)}{N} \) where \( N \) represents the number of bits in the sequence, and \( p \) represents the mean value of the number. For long word-lengths, a binomial random variable behaves as a Gaussian random variable. The mean and variance of a two-input stochastic logic gate are dependent on the bit-level correlation of the two inputs. This paper derives closed-form expressions for mean and variance of two-input stochastic logic gates with correlated inputs. An approach to synthesize correlated stochastic bit streams with specified correlation from uncorrelated bit streams is also presented. Using the proposed synthesis method, stochastic logic gates are simulated with correlated inputs. The simulated values of means and variances are shown to be the same as the theoretical values; thus, the closed-form expressions are validated.

I. INTRODUCTION

Stochastic Computing (SC) was proposed in 1967 by Gaines [1] [2]. SC was proposed as an alternative approach to binary computing. SC uses a unary system as opposed to a weighted system. A number is represented by a string of 1’s and 0’s where each bit is assumed to be independent of the other bits, i.e., the bits are assumed to be random. This randomness corresponds to temporal independence, i.e., the bits at different positions (or times) are uncorrelated. Closed-form expressions for stochastic logic outputs have been derived for uncorrelated inputs in [10]. Synthesis of logic gates to compute specified probabilities from uncorrelated bit streams has been proposed in [11] [12]. However, the bit-level correlation between the two inputs to a stochastic logic gate affects the expected value of the output. Recently, the notion of stochastic correlation has been introduced in [13] and has been used to generate correlated bit streams using probabilistic transfer matrices. In contrast, the proposed work presents a method to generate correlated bit streams using Pearson correlation. Although the Pearson correlation coefficient, \( \rho \), lies between -1 and 1, the \( \rho \) of two stochastic bit streams is restricted to a narrower range; this range is dependent on the expected values of the stochastic inputs.

This paper makes two key contributions. First, closed-form expressions are derived for mean and variance of outputs of two-input stochastic logic gates as functions of the input probabilities and the spatial correlation between the inputs. To prove the theoretical expressions by simulations, it is necessary to generate correlated bit streams for a specified correlation. However, generation of correlated stochastic bit streams has not been addressed in prior work. The second contribution of this paper is a novel approach to generate correlated bit streams. Finally, the validity of the theoretical expressions is demonstrated through simulations of stochastic logic gates using correlated bit streams.

This paper is organized as follows. In Section II closed-form expressions for outputs of stochastic logic gates with correlated inputs are derived. Section III presents an approach to synthesize correlated stochastic bit streams from uncorrelated bit streams. Section IV compares stochastic outputs computed theoretically and from simulations.

II. ANALYSIS OF STOCHASTIC LOGIC WITH CORRELATED INPUTS

Each input bit of a stochastic bit stream is assumed to be an independent identically distributed (IID) Bernoulli random variable with the probability of one equal to \( p \). Thus, the stochastic number is represented by a Binomial random variable with variance, \( \sigma^2 = \frac{p(1-p)}{N} \) where \( N \) represents the
number of bits in the word. Thus, the variance is maximum at \( p = 0.5 \) and is minimum at \( p = 0 \) or \( p = 1 \).

\[
\begin{array}{l}
0.5 \quad 100110 \\
0.333 \quad 001010 \\
0.166 \quad 000010
\end{array}
\]

Fig. 1: An example of multiplication using an AND gate

Correlation in bit streams alters the expected output of a stochastic logic circuit from that with independent bit streams. This will be discussed further in this section. Consider the multiplication of two stochastic numbers, \( X_1 \) and \( X_2 \) using an AND gate as shown in Figure 1. The probabilities of the two bit streams, denoted as \( p_1 \) and \( p_2 \), are assumed to be 0.5 and 0.3333, with word-length of 6 bits. Let \( Y \) denote the output. If \( X_1 \) and \( X_2 \) are uncorrelated, the output probability is given by \( E(Y) = p_1 \times p_2 \). In this example the output value is 0.1666. If the bits of the two inputs are correlated, the expected value of the output can be derived from the definition of the bit-level correlation coefficient:

\[
\rho = \frac{E(Y) - p_1 p_2}{\sigma_1 \sigma_2}
\]  

where \( p_1 \) and \( p_2 \) represent the mean values of the two stochastic inputs \( X_1 \) and \( X_2 \), and \( \sigma_1 \) and \( \sigma_2 \), respectively, represent the bit-level standard deviations of \( X_1 \) and \( X_2 \). The expected value of the output, \( Y \), is given by:

\[
E(Y) = E(X_1 X_2) = p_1 p_2 + \rho \sigma_1 \sigma_2 = p_1 p_2 + \rho \sqrt{p_1 p_2 (1 - p_1)(1 - p_2)}
\]

If the two bit-streams, \( X_1 \) and \( X_2 \) are identical, then \( p_1 = p_2 \) and \( \rho \) is one, and \( E(Y) = p_1 = p_2 \).

Consider a two-input OR gate with uncorrelated inputs. The mean value of its output is given by \( p_1 + p_2 - p_1 p_2 \) where \( p_1 \) and \( p_2 \), respectively, represent the expected values of \( X_1 \) and \( X_2 \). If \( X_1 \) and \( X_2 \) are correlated with correlation coefficient \( \rho \), using (1), the mean output of the OR gate can be calculated as:

\[
E(Y) = E(X_1 + X_2 - X_1 X_2) = p_1 + p_2 - p_1 p_2 - \rho \sigma_1 \sigma_2.
\]

The expected output of an XOR gate can be similarly computed as:

\[
E(Y) = p_1 + p_2 - 2p_1 p_2 - 2\rho \sigma_1 \sigma_2.
\]

The output of a MUX is unaffected by correlation of input signals. Let the input signals be denoted as \( X_1 \) and \( X_2 \), and the select signal be denoted as \( X_3 \). Let the stochastic values of these three signals be, respectively, given by \( p_1, p_2, \) and \( p_3 \). The mean output of the MUX, \( Y \) is given by:

\[
E(Y) = p_1 - p_1 p_3 + p_2 p_3.
\]

Although the mean output is unaffected by correlation between \( X_1 \) and \( X_2 \), it can be affected by the correlation between the control signal, \( X_3 \), and either or both input signals, \( X_1 \) or \( X_2 \).

The mean outputs of other stochastic logic gates can be derived in similar manner. Table I lists the mean outputs of various stochastic logic gates without and with input correlation.

### III. Synthesizing Correlated Bit Streams

To verify the results of Table I, it is necessary to synthesize two correlated bit streams for specified mean values and correlation coefficient. An approach to synthesize correlated stochastic bit streams from uncorrelated bit streams is presented in this section.

Let \( p_1, p_2 \) and \( \rho \), respectively, represent the mean values of stochastic numbers \( X_1, X_2 \), and their bit-level correlation coefficient. A joint probability mass function (pmf) of \( X_1 \) and \( X_2 \) is described in Table II, where the only unknown is \( a \). The parameter \( a \) describes the probability that \( X_1 = 1 \) and \( X_2 = 1 \), and can be derived from the correlation coefficient, \( \rho \).

<table>
<thead>
<tr>
<th>Input Signal</th>
<th>Probability</th>
</tr>
</thead>
<tbody>
<tr>
<td>( x_1 = 0, x_2 = 0 )</td>
<td>( 1 - p_1 - p_2 + a )</td>
</tr>
<tr>
<td>( x_1 = 0, x_2 = 1 )</td>
<td>( p_2 - a )</td>
</tr>
<tr>
<td>( x_1 = 1, x_2 = 0 )</td>
<td>( p_1 - a )</td>
</tr>
<tr>
<td>( x_1 = 1, x_2 = 1 )</td>
<td>( a )</td>
</tr>
</tbody>
</table>

Since all values in Table II represent probabilities, these must be non-negative. This is guaranteed by the constraints:

- \( a > 0 \)
- \( a < p_2 \)
- \( a < p_1 \)
- \( a > p_1 + p_2 - 1 \)

From the definition of the bit-level correlation coefficient, \( \rho \), given by:

\[
\rho = \frac{a - p_1 p_2}{\sigma_1 \sigma_2}
\]

the parameter \( a \) can be obtained as:

\[
a = p_1 p_2 + \rho \sigma_1 \sigma_2
\]

\[
= p_1 p_2 + \rho \sqrt{p_1 p_2 (1 - p_1)(1 - p_2)}.
\]

Note that although the correlation coefficient, \( \rho \), lies between \(-1\) and \(1\), the above constraints limit the allowable range of \( \rho \). For example, if \( p_1 = 0.3 \), and \( p_2 = 0.8 \), the range of \( a \) is constrained to the range \([0.1, 0.3]\). This limits the range of \( \rho \) to \([-0.7638, 0.3273]\).

The two correlated stochastic bit streams, \( X_1 \) and \( X_2 \), can be synthesized from two uncorrelated bit streams, denoted as \( R_1 \) and \( R_2 \), where each bit of \( R_1 \) and \( R_2 \) is a uniform random variable between 0 and 1. The proposed approach makes use
of marginal probability and conditional marginal probability. First $R_1$ is used to generate $X_1$ using marginal probability of $X_1$. Then, $X_2$ is generated from $R_2$ using conditional marginal probability of $X_2$ conditioned to selection of $X_1$. The approach to generating $X_1$ follows the principle of stochastic number generator (SNG). If the probability of first uncorrelated bit stream, $R_1$, is greater then $p_1$, then $X_1 = 0$, otherwise $X_1 = 1$. $X_2$ is synthesizes by using the conditional probability of $X_2$ given $X_1$, which is:

$$ P(X_2|X_1) = \frac{P(X_1, X_2)}{P(X_1)}. \quad (7) $$

Assume that $X_1 = 1$ is given, we obtain $P(X_2 = 1|X_1 = 1) = a/p_1$. If $R_2 > a/p_1$, then $X_2 = 0$. Otherwise, $X_2 = 1$. Given that $X_1 = 0$ is generated, the conditional probability will be $P(X_2 = 0|X_1 = 0) = (p_2 - a)/(1 - p_1)$. Then $X_2 = 0$ if $R_2 > (p_2 - a)/(1 - p_1)$. Otherwise $X_2 = 1$. Figure 2 shows the decision tree to synthesize two correlated stochastic bit streams with specified $p_1$, $p_2$, and $\rho$. Every bit of two stochastic sequences is generated using this decision tree.

IV. SIMULATION RESULTS

Stochastic bit streams with and without correlation are input stochastic logic gates. The difference in their outputs is referred as Deviation $D$. Using Monte Carlo experiments, a histogram of $D$ is constructed and its mean and standard deviation are obtained from simulation. These are then compared with theoretical values predicted from Table I.

TABLE III: Error Analysis

<table>
<thead>
<tr>
<th>Gate type</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND</td>
<td>$\rho_1 \sigma_2$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\rho_1 \sigma_2$</td>
</tr>
<tr>
<td>OR</td>
<td>$\rho_1 \sigma_2$</td>
</tr>
<tr>
<td>NOR</td>
<td>$\rho_1 \sigma_2$</td>
</tr>
<tr>
<td>XOR</td>
<td>$2\rho_1 \sigma_2$</td>
</tr>
<tr>
<td>XNOR</td>
<td>$2\rho_1 \sigma_2$</td>
</tr>
</tbody>
</table>

The mean values of the deviation for each gate are shown in Table III. This deviation is found by subtracting expected values with correlation from without using Table I. The standard deviation can be computed as a function of the length of the bit stream. Consider an AND gate as an example. Let the two mean values be given by 0.4 and 0.5 and the correlation coefficient be given by 0.2. The mean value of the output is simulated with and without correlation for a word-length of 100 bits with 2000 Monte Carlo runs. Figure 3 illustrates the histogram of the output value for correlated inputs.

![Fig. 3: The histogram for a 100 bits and 2000 experiments for independent bit streams.](image1)

The expected output for the AND gate with correlated inputs is given by:

$$ \hat{y} = p_1 p_2 + \rho \sigma_1 \sigma_2 = 0.2 + 0.2 \times \sqrt{0.4 \times 0.5} \times \sqrt{0.6} \times \sqrt{0.5} \quad \text{100} = .2489 $$

Using (8):

$$ E(\text{Deviation}) = \hat{y} - y = .2489 - .2 = .0489 \quad (8) $$

This can also be written as:

$$ E(\text{Deviation}) = p_1 p_2 + \rho \sigma_1 \sigma_2 - p_1 p_2 = \rho \sigma_1 \sigma_2 \quad (9) $$

The standard deviation of the Deviation can be calculated using $\sqrt{p(1-p)/N}$ using $p = 0.2489$ and $N = 100$, and is given by 0.0432. The Deviation histogram is shown in Fig. 4. This histogram is in agreement with the predicted value.
V. ANALYSIS OF TWO-LEVEL STOCHASTIC LOGIC

This section illustrates theoretical computation of mean output of two-level stochastic logic circuits with correlated inputs. Consider the two-level stochastic logic example shown in Figure 5. In this figure, $X_2$ is a common input to the two AND gates in the first level. We also assume $x_2$ to be independent of $x_1$ and $x_3$. Let $x_1$ and $x_3$ be correlated with a correlation coefficient $\rho$. Let $X_1$, $X_2$, and $X_3$ have probabilities of $p_1$, $p_2$, and $p_3$, respectively. Using Figure 5, we can find the $E(Z)$ by the following derivation:

$$E(Y_1) = E(X_1 X_2) = p_1 p_2$$
$$E(Y_2) = E(X_2 X_3) = p_2 p_3$$

Using the equation for the output of the AND gate with correlation:

$$E(Z) = E(Y_1 Y_2)$$
$$= p_1 p_2^2 p_3 + \rho \sqrt{p_1 p_2^2 p_3 (1 - p_1 p_2)} (1 - p_2 p_3)$$
$$= p_2 \left( p_1 p_2 p_3 + \rho \sqrt{p_1 p_2^2 p_3 (1 - p_1 p_2)} (1 - p_2 p_3) \right)$$

Note that the bit-level correlation between $Y_1$ and $Y_2$ is given by $\rho_{Y_1 Y_2}$. It can be shown that:

$$\rho_{Y_1 Y_2} = \frac{p_1 p_3 (1 - p_2) + \rho \sqrt{p_1 p_2 p_3 (1 - p_1 p_2)} (1 - p_2 p_3)}{\sqrt{p_1 p_3 (1 - p_1 p_2)} (1 - p_2 p_3)}$$

Further note if $\rho$ is 0, then $E(Z) = p_1 p_2 p_3$. Fig. 6 shows a circuit that is equivalent to Fig. 5.

For Figure 6, $E(Z)$ can be computed as follows:

$$E(Y_1) = p_1 p_3 + \rho \sqrt{p_1 p_2 p_3 (1 - p_1) (1 - p_3)}$$
$$E(Z) = E(X_2 Y) = p_2 (p_1 p_3 + \rho \sqrt{p_1 p_2 p_3 (1 - p_1) (1 - p_3)})$$

If $\rho$ is 0, then $E(Z) = p_1 p_2 p_3$.

VI. CONCLUSION

This paper has presented closed-form expressions for mean values of two-input stochastic logic gates with correlated inputs. A method to generate two correlated bit streams has been presented. Simulation results using synthesized correlated bit streams validate the theoretical expressions derived for the mean and variance values. Future work will be directed towards derivation of mean values of three-input logic gates, and for multi-level stochastic logic.

VII. ACKNOWLEDGMENT

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